

18/712808



S P E C I F I C A T I O N

Docket No. 93-C-20C1

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN that we, Tsiu Chiu Chan and Frank Randolph Bryant, citizens of the United States of America, residing in the State of Texas, have invented new and useful improvements in a

STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

of which the following is a specification:



08/712808

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation in part of an
application entitled "METHOD OF MAKING TRANSISTOR DEVICES
IN AN SRAM CELL", Serial No. 08/390,117, filing date
February 17, 1995, which is a divisional of Serial No.
08/159,462 filed November 30, 1993, now US 5426065.

Applicant incorporates said application Serial No.
08/159,462 by reference herein and claims the benefit of
said application for all purposes pursuant to 37 C.F.R. §
1.78.

11 BACKGROUND OF THE INVENTION

12 1. Field of the Invention:

13 The present invention relates to integrated circuit
14 devices and more specifically to field effect transistors
15 (FET) for use in integrated circuits.

16 2. Description of the Prior Art:

17 Memories are devices that respond to operational
18 orders, usually from a central processing unit. Memories
19 may store large quantities of information in a digital
20 format. In a memory system or unit, addresses are used to
21 access the contents of the memory unit. A binary digit,
22 also called a bit, is the basic information element stored
23 in a memory unit. The smallest subdivision of a memory
24 unit into which a bit of information can be stored is
25 called a memory cell. A memory on a chip is physically
26 arranged as a two-dimensional array of cells, wherein rows
27 of cells are connected by row lines, also called word
28 lines. A column of cells are connected by a column line,
29 also called a bit line. These memory cells may be
30 constructed by various configurations of transistors and/or
31 capacitors.

32 A semiconductor memory is a memory that is implemented
33 in a semiconductor material such as silicon. Metal-oxide

1 semiconductor (MOS) memories are common in the industry.
2 A number of different types of MOS memories exist, such as
3 a dynamic random access memory (DRAM) which is a metal
4 oxide semiconductor memory that stores a bit of information
5 as a charge on a capacitor, and a static random access
6 memory (SRAM) which includes a bistable flipflop circuit
7 requiring only a DC voltage applied to it to retain its
8 memory. Normally, an SRAM contains four transistors plus
9 either two transistors or two polysilicon load resistors as
10 pull-up devices.

11 SRAMs have a disadvantage over a memory such as a
12 DRAM. The components in an SRAM typically require the SRAM
13 to have a larger basic cell than a DRAM. In SRAM memory
14 cells, the data transfer gate transistor to pull-down
15 transistor ON resistance ratio is typically required to be
16 about 2.6x or greater to provide stability to the memory
17 cell. Currently, the width of the pull-down transistor is
18 required to be larger than the width of the transfer gate
19 transistor to achieve the ratio requirement. This
20 requirement places limitations on how small the memory cell
21 may be made. Therefore, it would be desirable to have a
22 transistor structure that would allow for a reduction in
23 the area that a memory cell requires.

SUMMARY OF THE INVENTION

An SRAM memory cell having first and second transfer gate transistors. The first transfer gate transistor includes a first source/drain connected to a bit line and the second transfer gate transistor has a first source/drain connected to a complement bit line. Each transfer gate transistor has a gate connected to a word line. The SRAM memory cell also includes first and second pull-down transistors configured as a storage latch. The first pull-down transistor has a first source/drain connected to a second source/drain of said first transfer gate transistor; the second pull-down transistor has a first source/drain connected to a second source/drain of said second transfer gate transistor. Both first and second pull-down transistors have a second source/drain connected to a power supply voltage node. The first and second transfer gate transistors each include a gate oxide layer having a first thickness, and the first and second pull-down transistors each include a gate oxide layer having a second thickness, wherein the first thickness is different from the second thickness.

1 **BRIEF DESCRIPTION OF THE DRAWINGS**

2 The novel features believed characteristic of the
3 invention are set forth in the appended claims. The
4 invention itself however, as well as a preferred mode of
5 use, and further objects and advantages thereof, will best
6 be understood by reference to the following detailed
7 description of an illustrative embodiment when read in
8 conjunction with the accompanying drawings, wherein:

9 **Figure 1** is a schematic diagram of an SRAM cell in which a
10 preferred embodiment of a present invention may be
11 implemented;

12 **Figure 2** is a layout of the SRAM cell depicted in Figure 1;

13 **Figures 3A-3E** are schematic cross-section views of a
14 transfer gate transistor and pull-down transistor in an
15 SRAM cell during processing; and

16 **Figures 4-13** are layout diagrams of an SRAM during
17 processing according to the present invention.

1 **DESCRIPTION OF THE PREFERRED EMBODIMENT**

2 The process steps and structures described below do
3 not form a complete process flow for manufacturing
4 integrated circuits. The present invention can be
5 practiced in conjunction with integrated circuit
6 fabrication techniques currently used in the art, and only
7 so much of the commonly practiced process steps are
8 included as are necessary for an understanding of the
9 present invention. The figures representing cross-sections
10 and layouts of portions of an integrated circuit during
11 fabrication are not drawn to scale, but instead are drawn
12 so as to illustrate the important features of the
13 invention.

14 **Figure 1** is a schematic diagram of an SRAM cell 2 in
15 which a preferred embodiment of the present invention may
16 be implemented. SRAM cell 2 includes transistors **TG1**, **TG2**,
17 **PD1**, and **PD2**. SRAM cell 2 also includes resistors **R1** and
18 **R2**. Transistors **TG1** and **TG2** are transfer gate transistors
19 in SRAM cell 2 while transistors **PD1** and **PD2** are pull-down
20 transistors. Resistors **R1** and **R2** are used as pull-up
21 devices.

22 Transistor **TG1** has a source/drain connected to bit
23 line A, and transistor **TG2** has a source/drain connected to
24 bit line B. Bit line B is a complement of bit line A. The
25 gates of transistors **TG1** and **TG2** are connected to word line
26 C. As can be seen, transistors **PD1** and **PD2** are connected
27 in a cross-coupled configuration. In addition, the
28 source/drain of transistor **TG1** and transistor **PD1** is
29 connected to one end of resistor **R1** while the source/drain
30 of transistor **PD2** and transistor **TG2** are connected to one
31 end of resistor **R2**. The other ends of resistors **R1** and **R2**
32 are connected to power supply voltage VCC while transistors
33 **PD1** and **PD2** each have a source/drain connected to power
34 supply voltage VSS.

1 Typically, the power supply voltage VCC is at a higher
2 voltage than power supply voltage VSS. In a typical SRAM
3 cell, transistors **PD1** and **PD2** typically have a width of
4 2.1μ and a length of 0.7μ . Transistors **PG1** and **PG2**
5 typically have a width of 0.9μ and a length of 0.8μ .

6 Referring now to **Figure 2**, a layout of SRAM cell 2
7 from **Figure 1** is depicted. SRAM cell 2 in **Figure 2**
8 includes word lines 6 and 8, which are poly 1 lines. Bit
9 lines 10 and 12 include bit line contacts 14a and 14b. In
10 addition, SRAM cell 2 also has shared contacts 16a and 16b.
11 Transistor **TG1** includes a gate 18. Transistor **TG1** has a
12 width W1 and a length L1. Similarly, transistor **TG2** has a
13 gate 20 and a width W2 and a length L2. Pull-down
14 transistor **PD1** includes gate 22 and has a width W3 and a
15 length L3; pull-down transistor **PD2** includes gate 24 and
16 has a width W4 and a length L4.

17 **Figures 3A-3E** are cross-section views of a transfer
18 gate transistor and a pull-down transistor according to the
19 present invention. Specifically, **Figure 3A** is a cross-
20 section view of a pull-down transistor 26, which includes
21 a substrate 30 that is typically a monocrystalline silicon
22 of a conventional crystal orientation known in the art.
23 Many features of the present invention are applicable to
24 devices employing semiconductor materials other than
25 silicon as will be appreciated by those of ordinary skill
26 in the art. Substrate 30 may be either a p-type substrate
27 or an n-type substrate. In the present illustrative
28 example, a p-type substrate is employed.

29 As can be seen in **Figure 3A**, a gate structure has been
30 formed, which includes gate oxide layer 32 and polysilicon
31 layer 34. Source drain regions 36 have been implanted into
32 substrate 30. Various types of implants may be employed;
33 for example, n-type impurities may be implanted into a p-
34 type substrate. Source drain regions 36 are n-type active

1 regions in the illustrated example. Lightly doped drain
2 (LDD), regions 38 are defined using sidewall oxide spacers
3 40 as known by those skilled in the art. Alternatively,
4 LDDs 38 and sidewall spacers 40 may be omitted.

5 Transfer gate transistor 28 in **Figure 3B** is at the
6 same processing step as pull-down transistor 26 in **Figure**
7 **3A**. After formation of the gate oxide 32 in **Figure 3A**, the
8 region in which transfer gate transistor 28 is to be formed
9 is masked off. Thus, no processing is performed in the
10 region of transfer gate transistor 28 while the rest of
11 pull-down transistor 26 is formed. As can be seen in this
12 portion of SRAM cell 4, a window 42 has been opened in
13 dielectric layer 44 exposing gate oxide layer 32.
14 Dielectric layer 44 is an oxide in this example. Next,
15 gate oxide layer 32 is etched away in **Figure 3C**, exposing
16 surface 46 of substrate 30. Thereafter, a new gate oxide
17 layer 48 is grown on surface 46 of substrate 30 in window
18 42, as shown in **Figure 3D**. This new gate oxide layer 48
19 preferably has a thickness less than that of the original
20 gate oxide layer 32.

21 Thereafter, the gate of pull-down transistor 28 is
22 formed as illustrated in **Figure 3E**. The gate of pull-down
23 transistor 28 includes gate oxide layer 48 and polysilicon
24 layer 50. Source/drains 52 also are implanted in substrate
25 30. Source/drains 52 include LDDs 54, which are again
26 defined using sidewall oxide spacers 56. The thickness of
27 gate oxide 32 is greater than the thickness of gate oxide
28 48. This type of processing is employed to create transfer
29 gate transistors and pull-down transistors with different
30 gate oxide thicknesses, which allows for a reduction in the
31 width of pull-down transistors in an SRAM cell.

32 Although the depicted embodiment illustrates
33 completely etching away the gate oxide of pull-down
34 transistor 28, then producing a gate oxide of the desired

1 thickness, other methods of producing different gate oxides
2 may be employed according to the present invention. For
3 example, a gate oxide layer may be grown for transfer gate
4 transistor 28 first, and then an additional gate oxide
5 layer can be grown on both pull-down transistor 26 and
6 transfer gate transistor 28 to produce gate oxide layers of
7 different thicknesses for each of the transistors.
8 Transfer gate transistor 28 is completely masked from
9 processing after completion, and remains in the form
10 depicted in **Figure 3A** during the various processing steps
11 applied to pull-down transistor 28 in **Figures 3B-3C**.

12 According to the present invention, a reduced width
13 pull-down transistor dimension may be employed by adjusting
14 the ratio of the gate oxide thickness between the transfer
15 gate transistors and the pull-down transistors in the SRAM
16 cell. The needed thicknesses of the two gate oxides may be
17 selected using the following equation:

T90X

$$18 \quad RATIO \leq \frac{TOX_{tg}}{TOX_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{VCC-Vt_{tg}}{VCC-Vt_{pd}}$$

19 where RATIO is the desired ratio of the transfer gate
20 transistor and the pull-down transistor, TOX_{tg} is the gate
21 oxide thickness of the transfer gate transistor, TOX_{pd} is
22 the gate oxide thickness of the pull-down transistor, W_{pd} is
23 the width of the pull-down transistor, L_{pd} is the length of
24 the pull-down transistor, W_{tg} is the width of the transfer
25 gate transistor, L_{tg} is the length of the transfer gate
26 transistor, Vcc is the upper power supply voltage, Vt_{tg} is
27 the threshold voltage of the transfer gate transistor, and
28 Vt_{pd} is the threshold voltage of the pull-down transistor.

29 In the depicted example, RATIO is 2.6, VCC is equal to
30 3.3 volts, Vt_{tg} is 0.9 volts with a back bias, and Vt_{pd} is
31 equal to 0.7 volts. If 0.5μ feature design rules are

1 utilized (L equal 0.5μ , W equal 0.6μ), the pull-down
2 transistor width is 1.56μ . If the pull-down gate oxide
3 thickness is 120\AA , a 36% reduction in pull-down transistor
4 width (1.0μ feature), will require a 134\AA transfer gate
5 oxide thickness. A 50% reduction in pull-down transistor
6 width (0.8μ feature) requires a 165\AA transfer gate oxide
7 thickness. By reducing the width (W_{pd}) of the pull-down
8 transistor, the overall area of SRAM cell may be reduced.

9 **Figures 4-13** are layout diagrams of an SRAM cell
10 during processing according to the present invention. In
11 **Figure 4**, SRAM cell 4 located on a wafer has been processed
12 and is ready for gate oxide. Active areas 100 have been
13 formed in the substrate of the wafer by growing a field
14 oxide everywhere else. Transfer gate oxide is grown on the
15 wafer and a poly 1 is deposited. In **Figure 5**, the poly 1
16 is patterned for transfer gate transistors in areas 102.
17 Drain/source implantation for the transfer gate transistors
18 is performed with resist patterns blocking implant into
19 pull-down transistor areas 104 in **Figure 6**. Thereafter, a
20 blanket threshold voltage adjust implant is performed for
21 the pull-down transistors. Then undoped oxide is deposited
22 on the wafer in a thickness of about 1000\AA . The undoped
23 oxide is removed in **Figure 7**. Undoped oxide in areas 106
24 are protected from removal with resist patterns to protect
25 the poly 1, which causes only those areas 104 intended for
26 the pull-down transistors to be exposed. The pull-down
27 transistor gate oxide is grown; a thin buffer of poly is
28 deposited in a layer of about 500\AA . In **Figure 8**, resist
29 patterns are utilized to open shared contacts in areas 108.
30 Then, poly plus polycide is deposited for poly 2.

31 In **Figure 9**, the poly 2 is patterned for pull-down
32 transistors and the Vss line as shown in areas 110 in
33 **Figure 9**. Drain/source implantation is then performed for
34 the pull-down transistors. Thereafter, a thin oxide is
35 deposited over the wafer in a layer of about 700\AA . A spin-

1 on-glass process is performed to create a glass layer of
2 about 700Å. This layer is cured and densified.
3 Thereafter, thin glass is deposited on the wafer in a layer
4 of about 700Å. In **Figure 10**, second shared contacts are
5 opened using resist patterns to protect the rest of the
6 SRAM cell from being opened. The second shared contacts
7 are opened in areas **112**. Then, undoped poly 3 is deposited
8 in a layer of about 700Å thick. In **Figure 11**, the poly 3
9 is patterned with resist to remain in areas **114**. This poly
10 layer will be used for the SRAM cell pull-up resistors, and
11 VCC supply lines. Undoped oxide is deposited in a layer of
12 about 1000Å on the wafer and a blanket implant for poly 3
13 is performed to set the poly resistor resistance on the
14 wafer. Thereafter, a n+ implant is performed for the VCC
15 portions of poly 3 utilizing a resist pattern covering
16 areas **116** in **Figure 12**. Contact windows are cut in areas
17 **118** in **Figure 13**.

18 Thus, the present invention provides a method and
19 structure for reducing the overall cell area of a memory
20 cell. The present invention provides an ability to reduce
21 the area of a memory cell by allowing the widths of the
22 pull-down transistors to be reduced. The reduction in
23 width is accomplished according to the present invention by
24 selecting different gate oxide thicknesses for the pull-
25 down transistor and the transfer gate transistor to
26 maintain the desired ratio.

27 Although the depicted embodiment defines specific
28 numbers for ratios, widths, lengths, in other parameters
29 may be utilized by those of ordinary skill in the art
30 following this disclosure. In addition, the different gate
31 oxide thicknesses for transistors in the SRAM memory cell
32 may be applied to other types of memory cells in which
33 widths or lengths of transistors can affect the area that
34 a cell requires.

1 While the invention has been particularly shown and
2 described with reference to a preferred embodiment, it will
3 be understood by those skilled in the art that various
4 changes in form and detail may be made therein without
5 departing from the spirit and scope of the invention.

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